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# Comprehensive dynamic on-resistance assessments in GaN-on-Si MIS-HEMTs for power switching applications

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**Abstract**

This study comprehensively analyzed the reliability of trapping and hot-electron effects responsible for the dynamic on-resistance (Ron) of GaN-based metal–insulator–semiconductor high electron mobility transistors. Specifically, this study performed the following analyses. First, we developed the on-the-fly Ron measurement to analyze the effects of traps during stress. With this technique, the faster one (with a pulse period of 20 ms) can characterize the degradation; the transient behavior could be monitored accurately by such short measurement pulse. Then, dynamic Ron transients were investigated under different bias conditions, including combined off state stress conditions, back-gating stress conditions, and semi-on stress conditions, in separate investigations of surface- and buffer-, and hot-electron-related trapping effects. Finally, the experiments showed that the Ron increase in semi-on state is significantly correlated with the high drain voltage and relatively high current levels (compared with the off-state current), involving the injection of greater amount of hot electrons from the channel into the AlGaN/insulator interface and the GaN buffer. These findings provide a path for device engineering to clarify the possible origins for electron traps and to accelerate the development of emerging GaN technologies.

Keywords: GaN MIS-HEMT, reliability, trapping related degradation, failure mechanisms, hot electrons, dynamic $R_{ON}$

(Some figures may appear in colour only in the online journal)

## 1. Introduction

The GaN properties and heterojunction technologies of GaN power HEMTs now enable high voltage (over 650 V) [1, 2], high power density (35 W in$^{-3}$) [3], high frequency (over 1 MHz) [3], and high temperature (up to 200 °C) operation [4]. Therefore, they can be used to improve power conversion in energy-efficient, smaller and more cost-effective products, such as power supplies, hybrid electric vehicles/electric vehicles [5, 6], and photovoltaic inverters [7]. Nevertheless, a relatively large amount of intrinsic defects and impurities still exist in the grown AlGaN/GaN hetero-structures which may act as charge traps (possibly causing the current collapse and increase in dynamic on-resistance $R_{on}$), and which thereby undermine the dynamic performance [8–10]. In more mature lateral GaN technology, dynamic switching problems still present a limitation on the market penetration of these devices. Several papers investigated the time resolved dynamic

[4] These authors contributed equally to this work.

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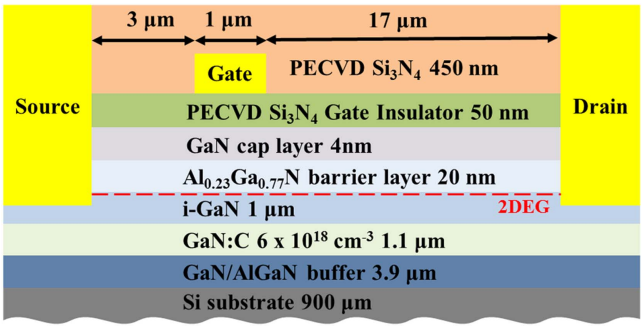


**Figure 1.** Schematic cross section of the fabricated MIS-HEMT device.

$R_{on}$ transients performed in off-state and back-gating stresses, suggesting the unique dominant trapping mechanisms related to the surface and to GaN buffer [11–13]. Conversely, systematic descriptions of the correlation of hot electrons-related charge-trapping and surface-state creation for devices stressed in semi-on state are rarely reported in the literature [14, 15]. Hot electrons-related charge-trapping play a major role in increasing the dynamic $R_{on}$ and promoting significant parasitic trapping effects (critical in hard switching conditions).

Therefore, this study comprehensively analyzed the main reliability concern for charge-trapping mechanisms in GaN-based MIS-HEMTs. The on-the-fly (OTF) technique is proposed to characterize trapping transients (increase in $R_{on}$ over time) for devices submitted to different bias regimes. This methodology is based on combined off state stress conditions, back-gating stress conditions, and semi-on stress conditions for separately investigating the surface- and buffer-, and hot-electron-related trapping processes. This study identified and described the dominant trapping mechanisms affecting the dynamic $R_{on}$: (i) in the off state condition, the trapping at the surface and in the buffer is promoted by high drain-gate bias ($V_{DG}$), (ii) in the back-gating condition, the trapping mostly occurs in the buffer, without any significant surface effect and is promoted by high vertical drain-to-substrate potential, (iii) in the semi-on condition, the injection of hot electrons from the channel into the AlGaN/insulator interface and the GaN buffer is caused by high drain voltage ($V_{DS}$) combined with high drain current ($I_{DS}$). These findings provide a path for device engineering to minimize degradation of dynamic on-resistance and to mature GaN into the robust technology.

## 2. Device description

Figure 1 shows the schematic cross-sectional view of the GaN MIS-HEMT in this study. The AlGaN/GaN HEMT structure was grown on 6 inch (111) p-type silicon substrate by metal-organic chemical vapor deposition. The epitaxial structure consisted of 4 nm GaN cap layer, 20 nm $Al_{0.23}Ga_{0.77}N$ barrier layer, 4 $\mu$m i-GaN layer, 1.1 $\mu$m GaN:C layer and the buffer layer consisted of GaN/AlGaN with total thickness of 3.9 $\mu$m. A 50 nm thick $Si_3N_4$ film was deposited by plasma-enhanced chemical vapor deposition and deployed as the gate insulator. Details on the Ohmic and gate contacts formation can be found in [16, 17], respectively. To clarify the origin of the degradation mechanism, the tested devices have no field plate (that has been proven to mitigate the large fields at the gate-drain and gate-source).

The device characterization was performed on devices with $L_{GD} = 17\ \mu$m, $L_{GS} = 3\ \mu$m, gate length $= 1\ \mu$m and gate width $= 50\ \mu$m. All devices were fabricated on the same 6 inch wafer and in close proximity to each other. Before starting with the evaluation of the origin of dynamic $R_{on}$, an initial survey of reliability qualification was performed to screen out early-stage degradation. These HEMT devices were preliminary subjected to direct current (DC) current–voltage ($I$–$V$) and off-state breakdown analyses with the aim of separating permanent degradation from trap-related phenomenon before any stress. Figures 2(a) and (b) show the representative results obtained from five identical samples. Characteristics of drain current ($I_{DS}$) versus drain voltage ($V_{DS}$) and gate voltage ($V_{GS}$) were recorded to determine the main DC device figures of merit, such as the linear-regime drain current $I_{Dlin}$ (measured at $V_{GS} = 0$ V and $V_{DS} = 1$ V), maximum drain current $I_{Dmax}$ (measured at $V_{GS} = 0$ V and $V_{DS} = 10$ V), on-resistance $R_{on}$ (defined as the inverse of $I_{Dlin}$), threshold voltage $V_{TH}$ (defined as $V_{GS}$ at $I_{DS} = 1$ mA for $V_{DS} = 1$ V) [18, 19]. Figures 2(c) and (d) show the drain and gate leakage currents ($I_{Doff}$ and $I_{Goff}$) measured in the voltage range from $V_{DS} = 0$ to 100 V with $V_{GS} = -25$ V (off-state). As can be noticed, the fabricated devices are able to sustain large drain biases ($V_{DS} > 100$ V) without the onset of a sudden increase of leakage current. Approximately 40 devices were evaluated and sorted to obtain well-matched $I$–$V$ characteristics.

Permanent and recoverable trapping and de-trapping effects may lead to significant increase in dynamic $R_{on}$. In order to clearly identify the effects on device characteristics, we have stressed these devices in the on state with $V_{DS} = 20$ V and $V_{GS} = 0$ V at room temperature which generates a constant heat into channel [9]. This is a harsh stress bias condition designed to accelerate the degradation rate and eventually permanent degradation in $R_{on.}$ During stress, we have characterized several device parameters by a benign characterization suite for a period of 300 s each. Figure 3 plots the time evolution of $R_{on}$ and $I_{Dmax}$ (normalized to their initial values) as well as $I_{Goff}$ as a function of stress time for the device that has been subject to 40 000 s. The device shows quite robust characteristics, during and after on state stress test, no sudden increase in gate leakage ($I_{Goff}$) is observed. In order to be able to separate permanent from trap-related degradation, the devices are exposed to ultraviolet illumination to fully de-trap the captured charge after stress [20, 21]. As figure 4 shows, the samples exhibit very minor degradation in their $R_{on}$ and $I_{Dmax}$ values, permanent degradation will still be small and its effect on device characteristics can be negligible.

## 3. OTF Ron characterization

A reliable and reproducible performance assessment of MIS-HEMT technology must not cause irreversible damage or irregular current behaviors. For this, the measurement

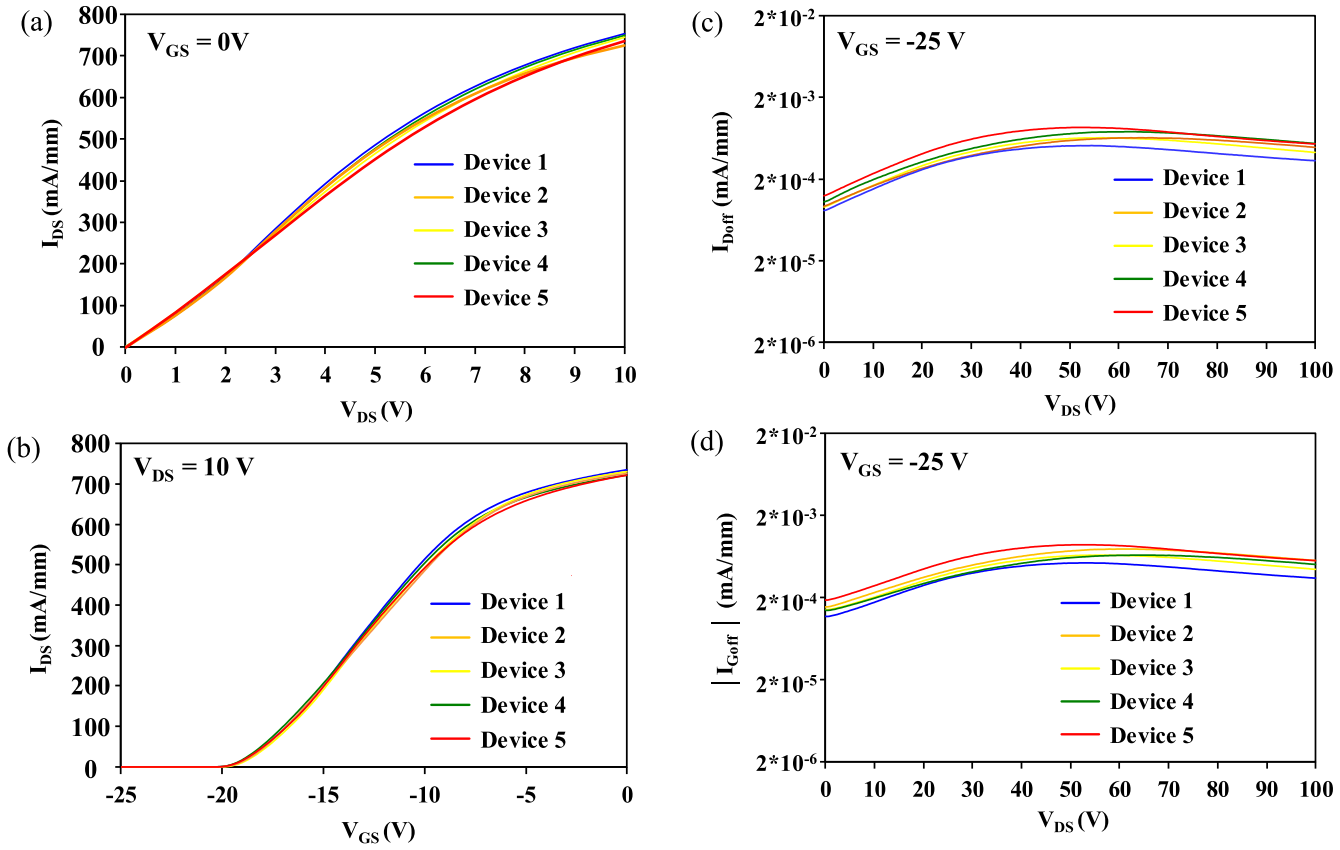


**Figure 2.** Representative device characteristics of MIS-HEMTs (five devices) used in this work. (a) Output ($V_{GS}$ = 0 V) characteristics measured at $V_{DS}$ from 0 to 10 V; (b) transfer ($V_{DS}$ = 10 V) characteristics measured at $V_{GS}$ from −25 to 0 V; (c) drain-leakage ($I_{Doff}$) characteristics measured at $V_{DS}$ from 0 to 100 V; (d) Gate-leakage breakdown ($I_{Goff}$) characteristics measured at $V_{DS}$ from 0 to 100 V. Negligible permanent degradation takes place as a result of the entire device characterization.

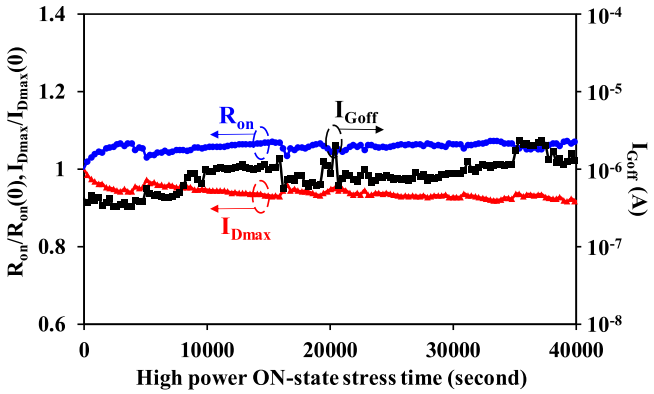


**Figure 3.** Time evolution of $R_{on}$ and $I_{Dmax}$ (normalized to their initial values) and $I_{Goff}$ during the devices are on-stressed at $V_{DS}$ = 20 V and $V_{GS}$ = 0 V. Small degradation in $R_{on}$ and $I_{Dmax}$, less than 10%, occur during this accelerated stress testing. No sudden increase in $I_{Goff}$ is observed.

conditions have to be selected carefully, so that the transient trapping/de-trapping effects can be studied in detail. The increase in dynamic $R_{on}$ is carried out by means of OTF transient characterization [22–24]. This technique is proposed to monitor the drain current ($I_{DS}$) degradation in stressed devices under off-state conditions. The main advantage of this technique is that the dynamics of trapped charge in transistors can be captured very shortly after the stress is removed.

The analysis is performed in an on-wafer probe station equipped with thermal chuck that allows device characterization through external test equipment (two Keithley 2636B Source Meters). Figure 5(a) is a schematic diagram of the experimental procedure for OTF $R_{on}$ transient characterization. Devices are kept in a defined trapping condition for 1000 s (for reliability assessment in different operating bias conditions, section 4); Stress-induced change in $R_{on}$ is evaluated by repeatedly biasing the device with short pulses (20 ms). Device $R_{on}$ is evaluated by averaging the sampled $I_{DS}$ values obtained from the measurement time interval (between 4 and 20 ms), retains sufficient accuracy to capture the transients. To further clarify the dynamic behavior, the correlation between specific trap formation and stress time for each cycle have been established to investigate the de-trapping effects during the characterization. Figure 5(b) shows the $R_{on}$ transients, which consist of a series of stress pulses with different stress times (1, 5, and 10 s) applied to a single device, and the change in Ron between pulses. During this measurement, the device is kept in the off-state bias ($V_{GS}$ = −25 V, $V_{DS}$ = 20 V, and $V_{SUB}$ = 0 V) for a long time (1000 s). Interestingly, a weak dependence of $R_{on}$ on the time the device is held in the OFF state; these pulses are significantly shorter than the de-trapping time of the defects. The $R_{on}$ did not substantially differ. Therefore, the device does not change its stress sequence (stressed 1 s for each

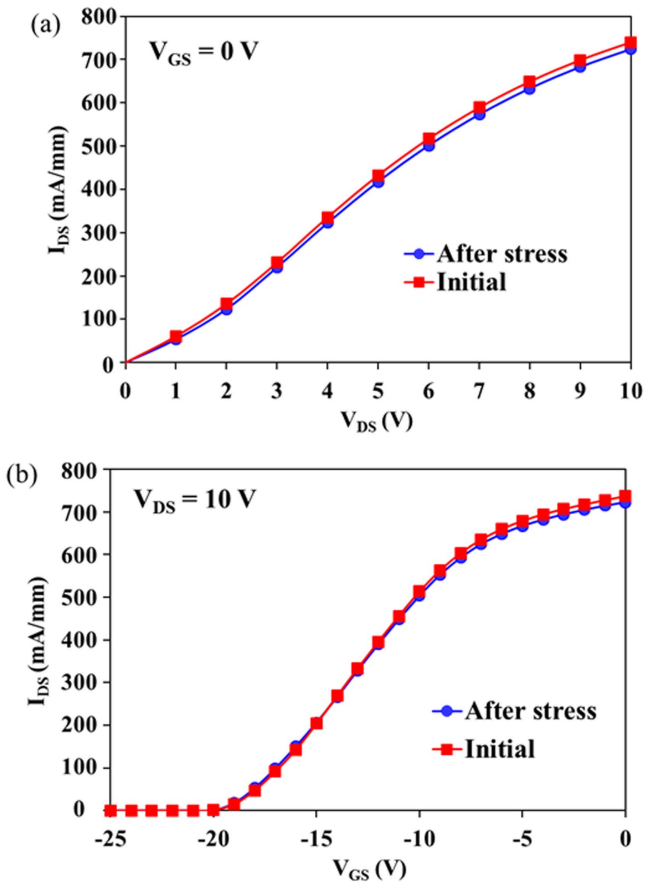


**Figure 4.** (a) Output ($V_{GS}$ = 0 V) and (b) transfer characteristics ($V_{DS}$ = 10 V) before and after on state stress. Negligible permanent $R_{on}$ and $I_{Dmax}$ happen.

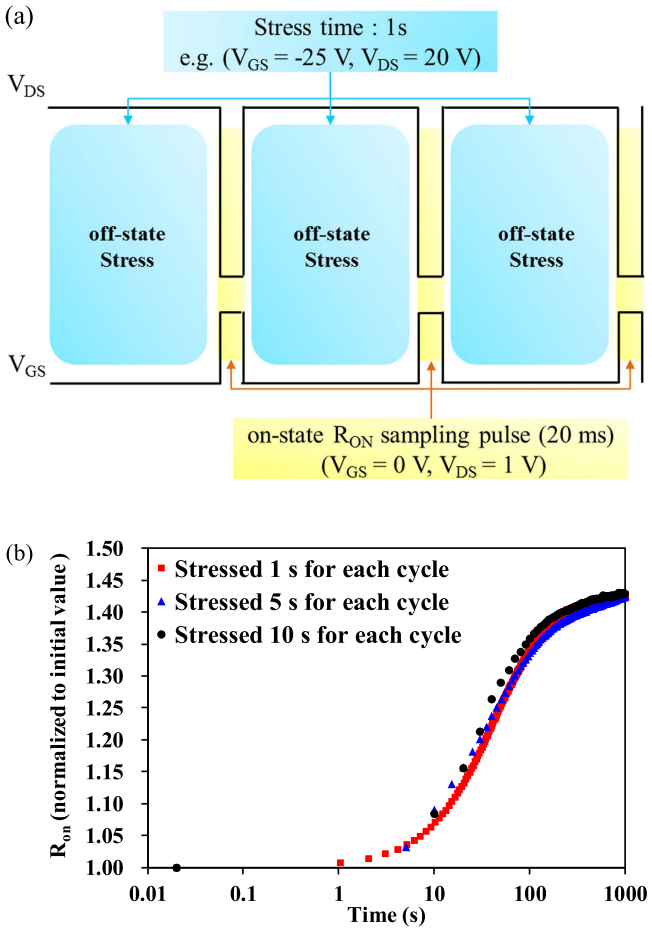


**Figure 5.** (a) The on-the-fly $R_{on}$ characterization involves holding a small bias on the drain and sampling the drain current continuously. This technique allows a few point sweep to be completed and the stress conditions returned in time interval of 20 ms. (b) the recorded $R_{on}$ transient is obtained by continuously switching the device between on-state ($V_{DS}$ = 1 V, $V_{GS}$ = 0 V, in linear region) and off-state ($V_{DS}$ = 20 V, $V_{GS}$ = −25 V for safety reason) for different periods of stress times (1, 5, and 10 s for each cycle).

cycle) during the short measurement pulse; this guarantees a reproducible and reliable evaluation of the $R_{on}$ time transients.

## 4. Trapping mechanisms in GaN-based MIS-HEMTs

Operation of the fabricated devices at a high drain bias increased $R_{on}$ over time. Figure 6 shows the schematic drawing of lateral and vertical trapping phenomena in MIS-HEMTs exposed to high drain bias. The increase in $R_{on}$ originates from increased injection of electrons from the gate-drain access regions (due to the high negative gate-drain voltage) and from the substrate to the buffer (due to the flow of drain-bulk vertical current). The physical origin of the mechanisms responsible for dynamic $R_{on}$ was investigated by analyzing trapping transients on devices starting at various quiescent bias points in the off-state, from $V_{DS}$ = 20 V to 100 in 20 V increments at $V_{GS}$ = −25 V, as shown in figure 7(a). When the evolution of normalized $R_{on}$ was reported as a function of time, an increase in stress voltage accelerated the trapping process and resulted in a stronger $R_{on}$ increase. These results suggest that the phenomena causing the $R_{on}$ temporary increase during time might be related to electron capture processes. Figure 7(b) reports the time constant spectra [25] extracted from $R_{on}$ transients in figure 7(a): the time constants are extrapolated by fitting the curves based on a stretched exponential function (black solid line in figure 7(a)); the derivative spectrum ($dR_{on}/d\log(t)$ waveform) for each tested has a clear peak, with relatively slow time constant (in the time interval of 10–70 s) [11, 13]. Remarkably, increasing drain potential yields a dramatic decrease in the time constant associated with the transient response.

The increased injection of electrons from the Si substrate to the buffer has a critical interaction with the performance and reliability of said devices. Mostly deep traps have been associated with early stages of degradation. Therefore, the effects of trapping in the buffer must be studied carefully. Furthermore, the back-gating measurement provides an effective method to distinguish between the surface- and buffer-related traps; this technique could offer a good indicator for process improvement. Figure 8 shows the devices stressed under back-gating bias at different negative substrate voltages ($V_{Sub}$ = −20 to −100 V with −20 V increments), with grounded source, gate and drain. The main mechanism of degradation is trapping in the buffer (high vertical field

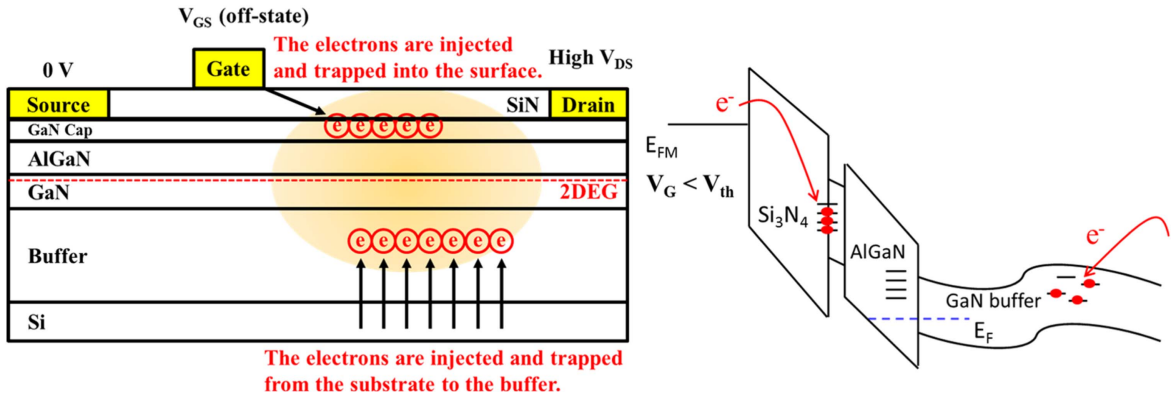


**Figure 6.** Schematic and band diagram representation of the possible trapping mechanisms of increased $R_{ON}$ in MIS-HEMTs exposed to high drain bias: electron trapping at both the surface (due to the electric field in the drain-gate access region) and in the buffer (due to the high vertical field from the drain directed towards the substrate).

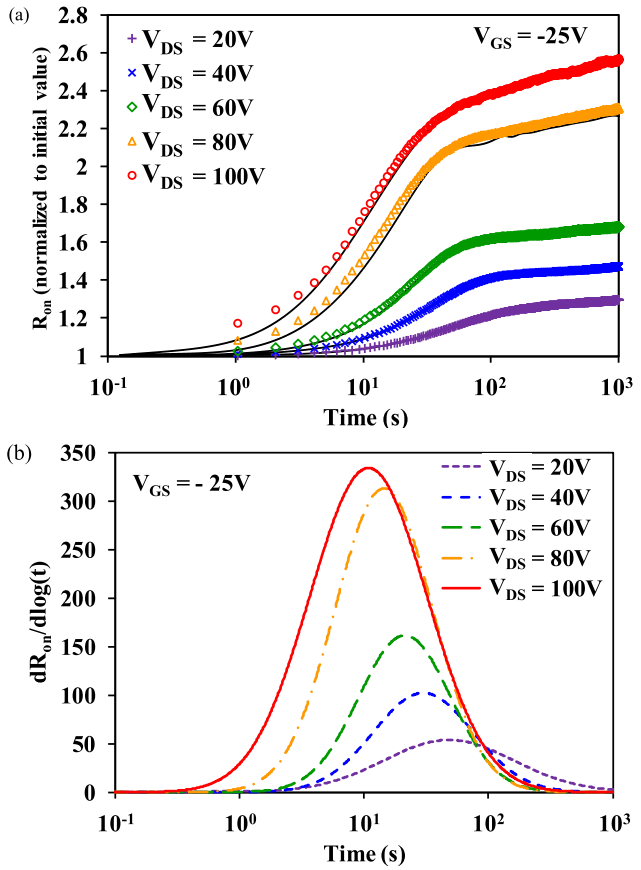


**Figure 7.** (a) $R_{ON}$ increase when the device was continuously pulsed under off state drain bias stresses; samples were subject to varying high drain-bias stress from $V_{DS}$ = 20–100 V at $V_{GS}$ = −25 V. (b) Time-constant spectra for $R_{ON}$ transients. A sum of exponential terms is used to fit the measurement data. High drain bias substantially increased the magnitude of transients with the related time constants (10–100 s).

between the channel and substrate), with negligible surface trapping (lateral field is zero between the three terminals) [26].

Dynamic $R_{on}$ measurements at different back-gating stress have been performed with the goal of clarifying the physical origin of these transients. Figure 9 shows $R_{on}$ transients and related time constant spectrum with different back-gating biases ($V_{sub}$) from −20 V to −100 V in −20 V step. As $V_{Sub}$ increases, $R_{on}$ increases exponentially over time. The time constant spectrum has a clear peak with a time constant in the range of 10–50 s. The dynamic $R_{on}$ increases in the devices presumably resulting from a depletion region forming within the GaN buffer. Also, electrons can be injected from the substrate to the buffer, eventually being trapped either in the buffer or in the GaN channel layer.

Substrate bias experiments are key performance indicators for distinguishing between surface- and buffer-related trapping processes. Notably, during back-gating stress, $R_{on}$ increases by approximately only 130% within the first 100 s of operation at 100 V and then flattens out. Furthermore, a very low drain-substrate leakage current was also observed during 300 V vertical bias supply as shown in figure 9(c). The well-controlled vertical GaN buffer leakage current has been shown to be able to suppress the trapping effects on the back gating stress operation [27]. Therefore, the weak Ron increased in figure 9(a) indicates that the substrate-related trapping process can effectively eliminated by the high quality GaN buffer structure in this study. Under off state stress operation, however, it shows a continuous increase in stress but does not saturate. The probable explanation for this behavior is that the surface traps have a determining factor for transient Ron variation characteristics compared to buffer traps.

This study also investigated the trapping mechanisms induced by the exposure to high semi-on state bias; it is important to evaluate the impact of the injection of hot electrons from the 2DEG into trap states to assess the stability of the devices. The semi-on bias condition is typically the worst case for hot-carrier stress. Notably, the additional traps filled in the semi-on condition are not present in off-state condition; strong correlation with hot-electron effects (see the schematic drawing of the trapping behavior in figure 10). When the device is biased in the semi-on state under a high current flow and high drain bias, in addition gate injection trapping process, the electrons in 2DEG channel are accelerated by the field and then injected in the AlGaN barrier defect or buffer near the channel.

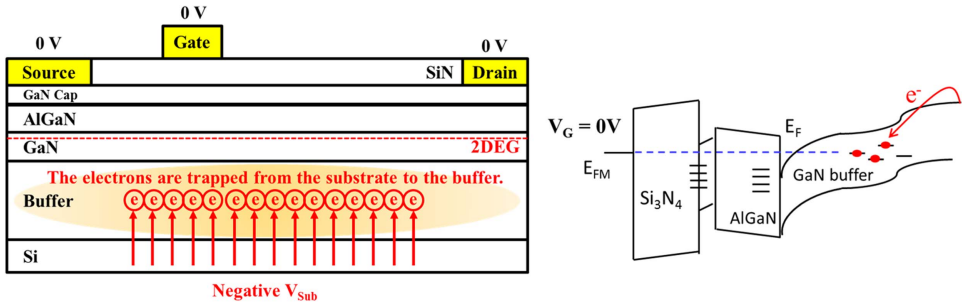


**Figure 8.** Schematic and band diagram representation of the possible trapping mechanisms responsible for $R_{ON}$-increase in MIS-HEMTs exposed to negative substrate bias ($V_{sub}$): the increased injection of electrons from the substrate to the buffer (due to the high vertical field).

This study further investigated the effects of hot electrons on device reliability. $R_{on}$ transients and related time constant spectra have been acquired by keeping the quiescent drain bias ($V_{DS}$ = 60 V) constant and by sweeping step-by-step the quiescent gate bias from $V_{GS} = V_{TH} - 5$ V (off-state) to $V_{TH} + 1$ V (semi-on state). Further, we also carried out experiments under a higher a quiescent bias point ($V_{DS} = 100$ V, $V_{GS} = V_{TH} + 1$ V) to investigate an increase of hot electron concentration.

Figure 11(a) shows that dynamic $R_{on}$ does not significantly change when exposed to the off-state quiescent bias ($V_{GS} < V_{TH}$). However, when the devices are biased in the semi-on state quiescent bias ($V_{GS} > V_{TH}$), the $R_{on}$ increase during semi-on (220% at $V_{DS} = 100$ V and $V_{GS} = V_{TH} + 1$ V) is higher than during off-state (160% at $V_{DS} = 60$ V and $V_{GS} = V_{TH} - 5$ V). The $R_{on}$ increase in the semi-on state is significantly correlated with the drain current. This suggests an additional trapping mechanism that is promoted by the high voltage ($V_{DS}$) and relatively high current levels (compared with the off-state current).

To ensure that the observed phenomenon only occurred in semi-on state operation, and to identify the possible trapping mechanism emerges, involving the injection of hot electrons, the time constant spectrum was extracted by acquiring the $R_{on}$ transients under off state and semi-on state stress. Figure 11(b) shows the experimental results, which indicate that, besides the trapping phenomena related to off-state operation (in the range of 10–30 s), an additional charge-trapping phenomena appears when the device is subjected to semi-on state bias stress (in the range of 600–800 s), and this observed trap signal is strongly correlated with drain current density and significantly increases with increasing drain bias from 60 to 100 V. This additional trapping mechanism can be ascribed to the presence of hot-electrons in the channel (see the schematic drawing in figure 10). Semi-on operation may occur in hard switching condition, when the gate bias is increased before the drain bias drops from saturation to linear region. The devices are simultaneously exposed to high drain voltage $V_{DS}$ (at the drain side edge of the gate electrode) and relatively high drain-current $I_{DS}$ (a large amount of electrons). These electrons are accelerated by the electric field and are injected from the channel into the buffer or into the gate-drain surface. These hot electrons may lead to parasitic generation which can promote not only additional charge-trapping phenomena but also hot electron-related long term degradation

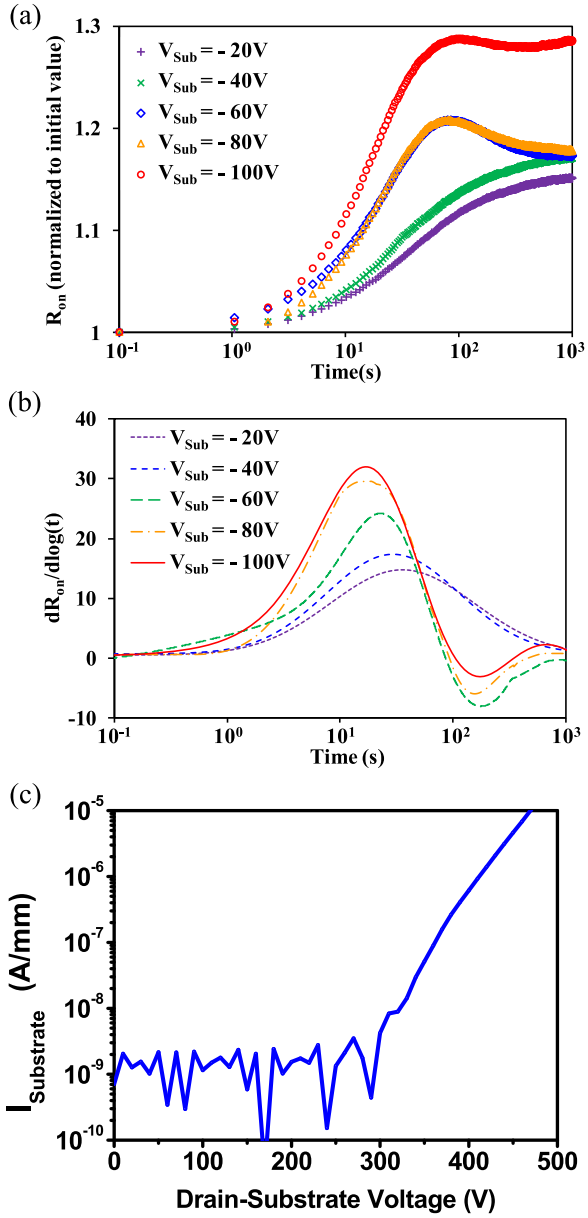


**Figure 9.** Recorded $R_{on}$ transients (a) and associated time constant spectrum (b) obtained from different quiescent $V_{Sub}$ conditions from $V_{Sub} = -20$ V up to $-100$ V in $-20$ V decrements. As $V_{Sub}$ increases, dynamic $R_{on}$ also increases, but the time constants do not significantly differ from those in figure 5(b). A clear positive peak appears in the said time constant signals; (c) substrate leakage current as a function of drain-substrate voltage.

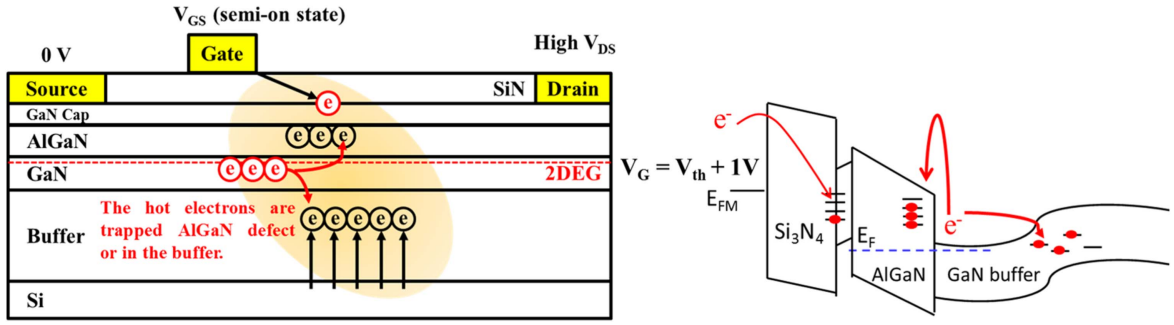


**Figure 10.** Schematic and band diagram representation of the additional possible trapping mechanisms responsible for the 'semi-on state' $R_{ON}$-increase in MIS-HEMTs exposed to high drain bias: the injection of hot electrons from the channel into the (SiN/GaN) interface and the GaN buffer layer.

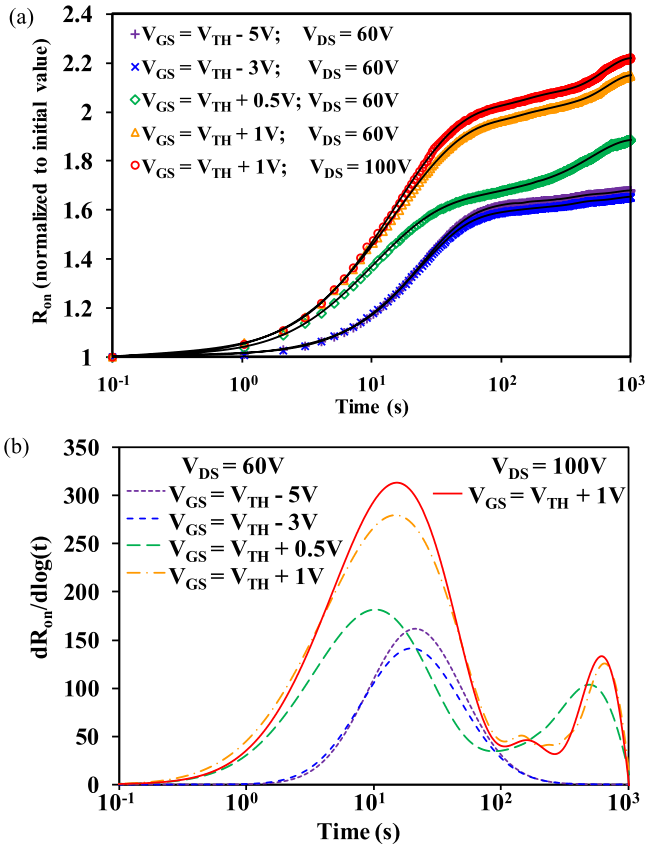


**Figure 11.** (a) Time-resolved $R_{on}$ transients acquired with constant quiescent $V_{DS}$ (60 V) and multiple quiescent $V_{GS}$ ($V_{TH}$ − 5 V to $V_{TH}$ + 1 V), in comparison with $R_{on}$ transient measured at quiescent bias point ($V_{DS}$ = 100 V, $V_{GS} = V_{TH}$ + 1 V; red line) to further characterize the hot-electron effects. Dynamic $R_{on}$ increase worsens as $V_{GS} > V_{TH}$. (b) During semi-on stresses, analysis of time constant waveforms showed an additional trap peak (in the time interval of 100–1000 s), which suggested a hot-electrons-related trapping mechanism.

effects ($R_{on}$ increases continuously as the device keeps on switching on and off).

## 5. Conclusion

This work investigated the three dominant charge-trapping effects affecting the dynamic increase of on-resistance ($R_{on}$) in GaN-based MIS-HEMT devices. The OTF trapping transient measurements revealed the following relevant results: (i) trapping of electrons at the surface and in the buffer, which is caused by off state with high drain-gate bias ($V_{DG}$); (ii) trapping in the buffer, without any significant surface effect, which is caused by back-gating operation with high vertical drain-to-substrate potential; (iii) trapping of hot electrons from the channel into the AlGaN/insulator interface and the GaN buffer, which is caused by the combination of high drain voltage ($V_{DS}$) and high drain current ($I_{DS}$) in the semi-on state. The origin of the traps, their location, and the physical mechanisms involved in the trapping are measured and statistically analyzed. Comparisons of the extracted time constant spectra revealed the underlying degradation mechanisms affecting device performance. Process/epitaxy improvements are necessary for GaN-based MIS-HEMTs to achieve stable and reproducible operation.

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